CD4018B Types

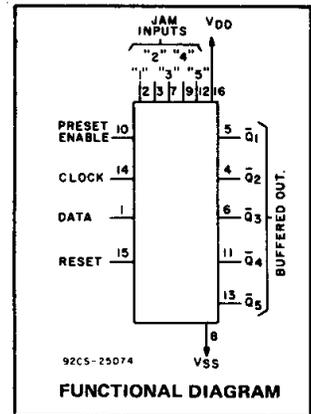## CMOS Presettable Divide-By-'N' Counter

High-Voltage Types (20-Volt Rating)

■ CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5; or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.
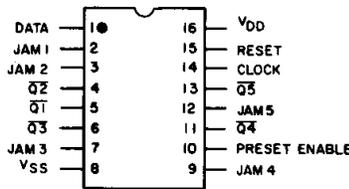
The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

■ Medium speed operation . . . . 10 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
■ Fully static operation
■ 100% tested for quiescent current at 20 V
■ Standardized, symmetrical output characteristics
■ 5-V, 10-V, and 15-V parametric ratings
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) =   1 V at V_{DD} = 5 V
                 2 V at V_{DD} = 10 V
                 2.5 V at V_{DD} = 15 V
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

FUNCTIONAL DIAGRAM

Applications:

■ Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
■ Fixed and programmable counters greater than 10
■ Programmable decade counters
■ Divide-by-"N" counters/frequency synthesizers
■ Frequency division
■ Counter control/timers

TERMINAL DIAGRAM
Top View

DATA — 1	16 — V_{DD}	
JAM 1 — 2	15 — RESET	
JAM 2 — 3	14 — CLOCK	
$\overline{Q2}$ — 4	13 — $\overline{Q5}$	
$\overline{Q1}$ — 5	12 — JAM 5	
$\overline{Q3}$ — 6	11 — $\overline{Q4}$	
JAM 3 — 7	10 — PRESET ENABLE	
V_{SS} — 8	9 — JAM 4	

92CS-24460

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) . . . . –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –55°C to +100°C 500mW
For T_A = +100°C to +125°C. . . . . Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING–TEMPERATURE RANGE (T_A). . . . . –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}). . . . . –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at $T_A = 25°C$, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Clock Input Frequency,	f_{CL}	5	–	3	
		10	–	7	MHz
		15	–	8.5	
Clock Pulse Width,	t_W	5	160	–	
		10	70	–	ns
		15	50	–	
Clock Rise & Fall Time,	t_rCL, t_fCL	5			
		10	Unlimited		μs
		15			
Data Input Set-Up Time,	t_S	5	40	–	
		10	12	–	ns
		15	16	–	
Data Input Hold Time,	t_H	5	140	–	
		10	80	–	ns
		15	60	–	
Preset or Reset Pulse Width,	t_W	5	160	–	
		10	70	–	ns
		15	50	–	
Preset or Reset Removal Time		5	160	–	
		10	60	–	ns
		15	40	–	
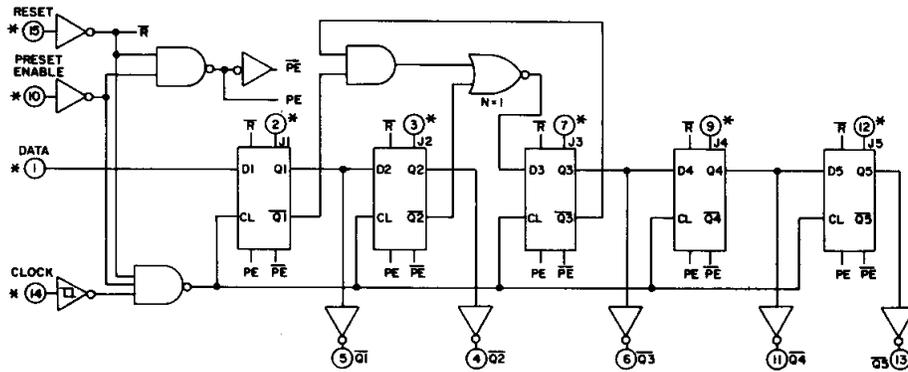
Fig. 1 – Logic diagram.
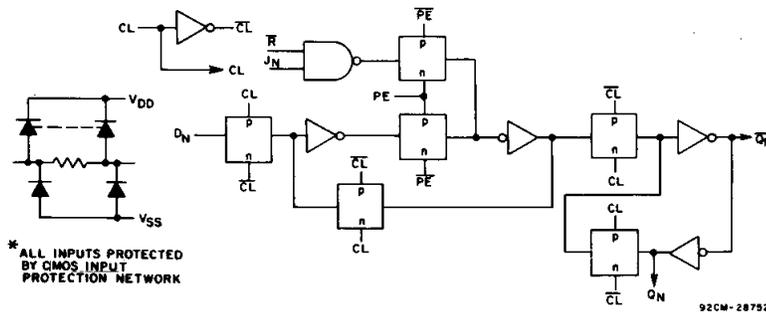
Fig. 2 – Detail of a typical stage.

CD4018B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-TERISTIC	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	−	0,5	5	5	5	150	150	−	0.04	5	μA
	−	0,10	10	10	10	300	300	−	0.04	10	
	−	0,15	15	20	20	600	600	−	0.04	20	
	−	0,20	20	100	100	3000	3000	−	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	−	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	−	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	−	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	−	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	−	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	−	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	−	
Output Voltage: Low-Level, V_{OL} Max.	−	0,5	5	0.05				−	0	0.05	V
	−	0,10	10	0.05				−	0	0.05	
	−	0,15	15	0.05				−	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	−	0,5	5	4.95				4.95	5	−	
	−	0,10	10	9.95				9.95	10	−	
	−	0,15	15	14.95				14.95	15	−	
Input Low Voltage V_{IL} Max.	0.5,4.5	−	5	1.5				−	−	1.5	V
	1,9	−	10	3				−	−	3	
	1.5,13.5	−	15	4				−	−	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	−	5	3.5				3.5	−	−	
	1,9	−	10	7				7	−	−	
	1.5,13.5	−	15	11				11	−	−	
Input Current I_{IN} Max.	−	0,18	18	±0.1	±0.1	±1	±1	−	±10^{-5}	±0.1	μA
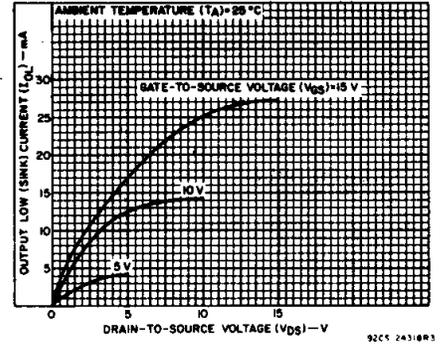
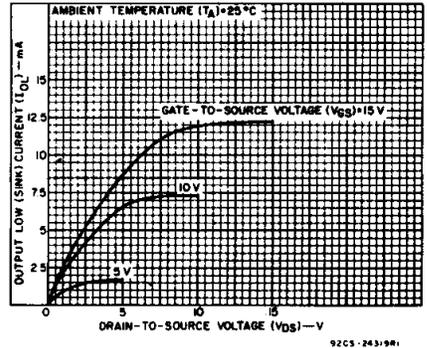Fig. 3 — Typical output low (sink) current characteristics.

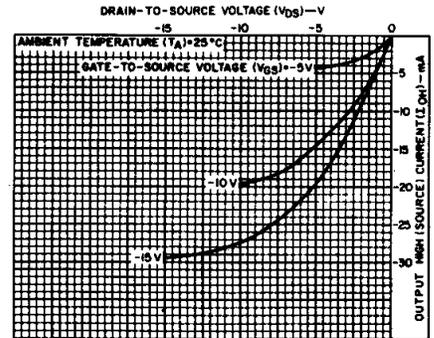Fig. 4 — Minimum output low (sink) current characteristics.

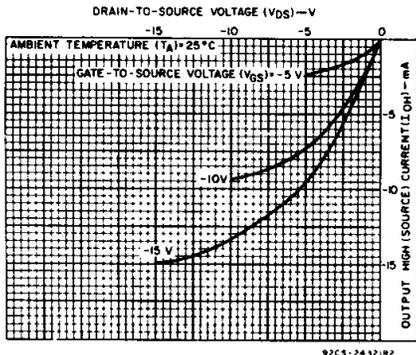Fig. 5 — Typical output high (source) current characteristics.

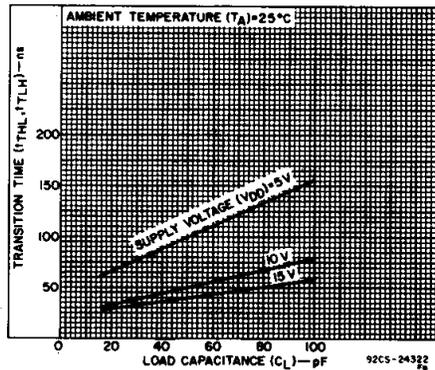Fig. 6 — Minimum output high (source) current characteristics.

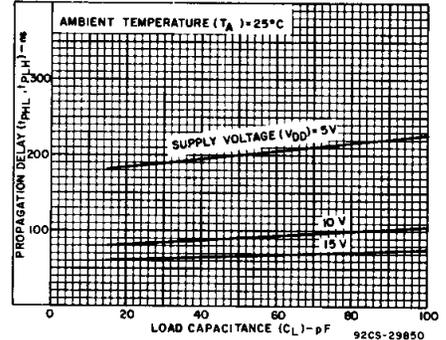Fig. 7 — Typical transition time as a function of load capacitance.

Fig. 8 — Typical propagation delay time as a function of load capacitance (CLOCK to Q).

DYNAMIC ELECTRICAL CHARATERISTICS at $T_A = 25°C$, Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
Propagation Delay Time;		5	—	200	400	
t_{PLH}, t_{PHL}		10	—	90	180	ns
		15	—	65	130	
Transition Time;		5	—	100	200	
t_{THL}, t_{TLH}		10	—	50	100	ns
		15	—	40	80	
Maximum Clock Input		5	3	6	—	
Frequency, f_{CL}		10	7	14	—	MHz
		15	8.5	17	—	
Minimum Clock Pulse Width,		5	—	80	160	
t_W		10	—	35	70	ns
		15	—	25	50	
Clock Rise & Fall Time;		5				
t_rCL, t_fCL		10		Unlimited		μs
		15				
Minimum Data Input Set-Up		5	—	20	40	
Time. t_S		10	—	6	12	ns
		15	—	3	6	
Minimum Data Input Hold		5	—	70	140	
Time, t_H		10	—	40	80	ns
		15	—	30	60	
Average Input Capacitance, C_I	Any Input		—	5	7.5	pF
PRESET* OR RESET OPERATION						
Propagation Delay Time;		5	—	275	550	
Preset or Reset to $\overline{Q}$		10	—	125	250	ns
t_{PLH}, t_{PHL}		15	—	90	180	
Minimum Preset or Reset		5	—	80	160	
Pulse Width,		10	—	35	70	ns
t_W		15	—	25	50	
Minimum Preset or Reset		5	—	80	160	
Removal Time		10	—	30	60	ns
		15	—	20	40	

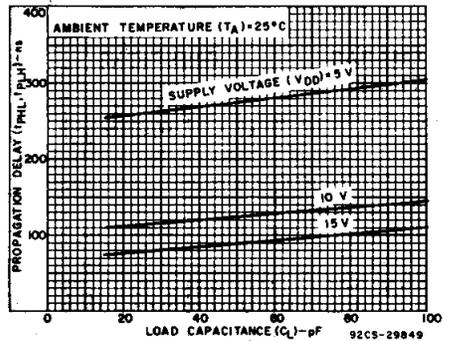* At PRESET ENABLE or JAM Inputs.

Fig. 9 — Typical propagation delay time as a function of load capacitance (RESET to Q).
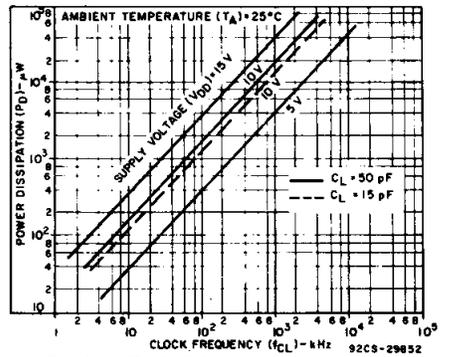

Fig. 10 — Typical dynamic power dissipation as a function of clock input frequency.
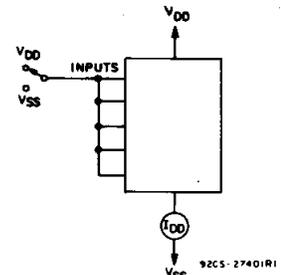

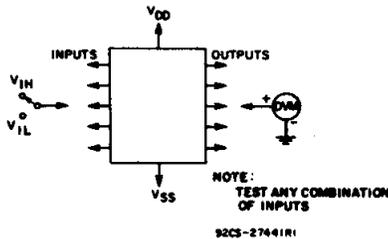Fig. 11 — Quiescent device current test circuit.
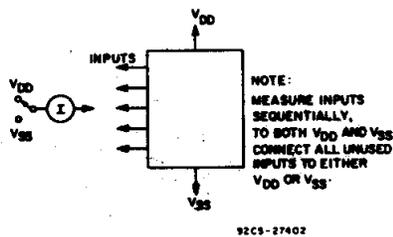

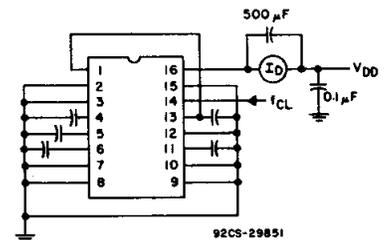Fig. 12 — Input voltage test circuit.

Fig. 13 — Input current test circuit.

Fig. 14 — Dynamic power dissipation test circuit.

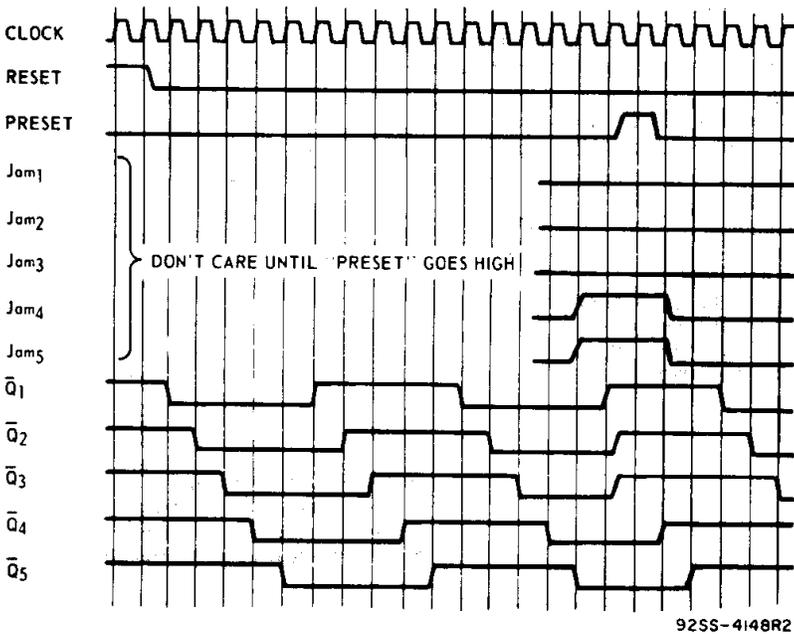("DATA" INPUT TIED TO $\bar{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

CLOCK
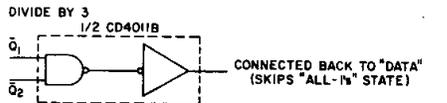RESET
PRESET
Jam$_1$
Jam$_2$
Jam$_3$
Jam$_4$
Jam$_5$
$\bar{Q}_1$
$\bar{Q}_2$
$\bar{Q}_3$
$\bar{Q}_4$
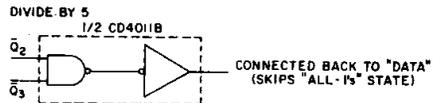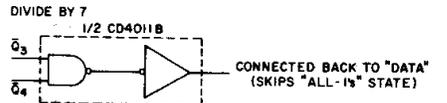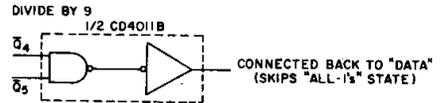$\bar{Q}_5$

DON'T CARE UNTIL "PRESET" GOES HIGH

92SS-4148R2

Fig. 15 — Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE
BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10	$\bar{Q}_5$		
DIVIDE BY 8	$\bar{Q}_4$	CONNECTED	NO EXTERNAL
DIVIDE BY 6	$\bar{Q}_3$	BACK TO	COMPONENTS
DIVIDE BY 4	$\bar{Q}_2$	"DATA"	REQUIRED
DIVIDE BY 2	$\bar{Q}_1$		

DIVIDE BY 9

1/2 CD4011B

$\bar{Q}_4$
$\bar{Q}_5$

CONNECTED BACK TO "DATA"
(SKIPS "ALL-1's" STATE)

DIVIDE BY 7

1/2 CD4011B

$\bar{Q}_3$
$\bar{Q}_4$

CONNECTED BACK TO "DATA"
(SKIPS "ALL-I's" STATE)

DIVIDE BY 5

1/2 CD4011B

$\bar{Q}_2$
$\bar{Q}_3$

CONNECTED BACK TO "DATA"
(SKIPS "ALL-I's" STATE)

DIVIDE BY 3

1/2 CD4011B

$\bar{Q}_1$
$\bar{Q}_2$

CONNECTED BACK TO "DATA"
(SKIPS "ALL-I's" STATE)

92CS-1707IR3

*Fig. 16 — External connections for divide by 10, 9,
8, 7, 5, 4, 3, 2 operation.*

85-93
(2.159-2.362)

4-10
(0.102-0.254)

77-85
(1.956-2.159)
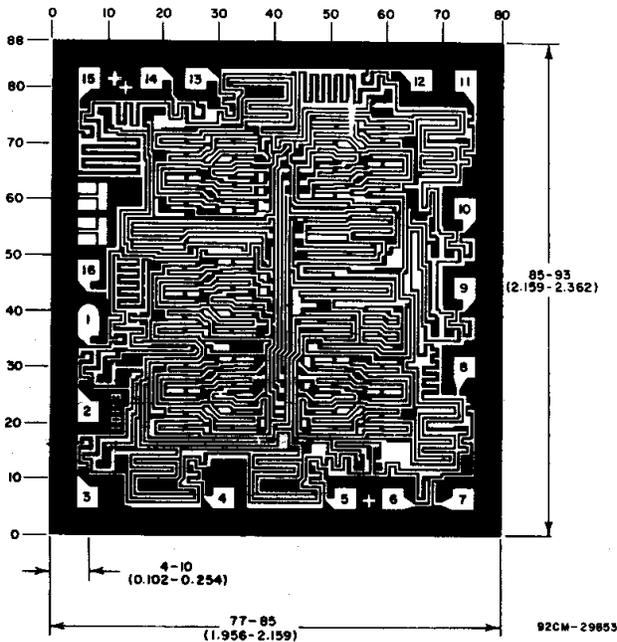
92CM-29853

Chip dimensions and pad layout for CD4018B

*Dimensions in parentheses are in millimeters and
are derived from the basic inch dimensions as in-
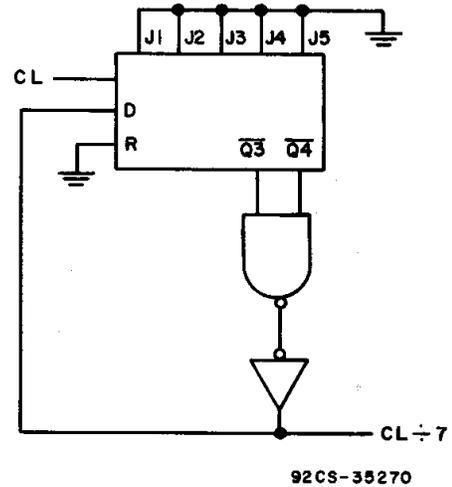dicated. Grid graduations are in mils (10^{-3} inch).*

J1 J2 J3 J4 J5

CL
D
R $\overline{Q3}$ $\overline{Q4}$

CL ÷ 7

92CS-35270

Fig. 17 — Example of divide by 7.

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