

8A, 500V, 0.850 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17425.

Ordering Information

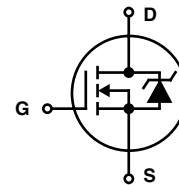
| PART NUMBER | PACKAGE | BRAND |
|-------------|----------|--------|
| IRF840 | TO-220AB | IRF840 |

NOTE: When ordering, include the entire part number.

Features

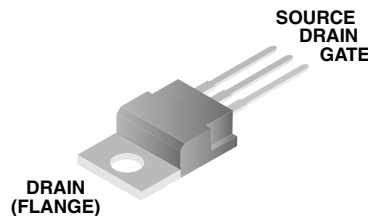
- 8A, 500V
- $r_{DS(ON)} = 0.850\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB
TOP VIEW



IRF840

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

| | IRF840 | UNITS |
|---|------------|---------------------|
| Drain to Source Voltage (Note 1) | 500 | V |
| Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) | 500 | V |
| Continuous Drain Current | 8.0 | A |
| $T_C = 100^\circ\text{C}$ | 5.1 | A |
| Pulsed Drain Current (Note 3) | 32 | A |
| Gate to Source Voltage | ± 20 | V |
| Maximum Power Dissipation | 125 | W |
| Linear Derating Factor | 1.0 | W/ $^\circ\text{C}$ |
| Single Pulse Avalanche Energy Rating (Note 4) | 510 | mJ |
| Operating and Storage Temperature | -55 to 150 | $^\circ\text{C}$ |
| Maximum Temperature for Soldering | | |
| Leads at 0.063in (1.6mm) from Case for 10s | 300 | $^\circ\text{C}$ |
| Package Body for 10s, See Techbrief 334 | 260 | $^\circ\text{C}$ |

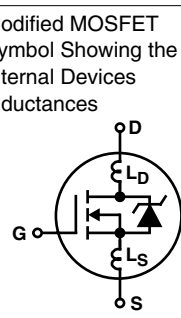
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|--|-----|------|-----------|--------------------|
| Drain to Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = 250 \text{ A}$ (Figure 10) | 500 | - | - | V |
| Gate to Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 250 \text{ A}$ | 2.0 | - | 4.0 | V |
| Zero-Gate Voltage Drain Current | I_{DSS} | $V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0V$ | - | - | 25 | A |
| | | $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0V, T_J = 125^\circ\text{C}$ | - | - | 250 | A |
| On-State Drain Current (Note 2) | $I_{D(ON)}$ | $V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10V$ | 8.0 | - | - | A |
| Gate to Source Leakage Current | I_{GSS} | $V_{GS} = \pm 20V$ | - | - | ± 100 | nA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $V_{GS} = 10V, I_D = 4.4A$ (Figures 8, 9) | - | 0.8 | 0.85 | Ω |
| Forward Transconductance (Note 2) | g_{fs} | $V_{DS} \geq 50V, I_D = 4.4A$ (Figure 12) | 4.9 | 7.4 | - | S |
| Turn-On Delay Time | $t_{D(ON)}$ | $V_{DD} = 250V, I_D \approx 8A, R_G = 9.1\Omega, R_L = 30\Omega$ MOSFET Switching Times are Essentially Independent of Operating Temperature. | - | 15 | 21 | ns |
| Rise Time | t_r | | - | 21 | 35 | ns |
| Turn-Off Delay Time | $t_{D(OFF)}$ | | - | 50 | 74 | ns |
| Fall Time | t_f | | - | 20 | 30 | ns |
| Total Gate Charge (Gate to Source + Gate to Drain) | $Q_{g(TOT)}$ | $V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{g(REF)} = 1.5mA$ (Figure 14) Gate Charge is Essentially Independent of Operating Temperature | - | 42 | 63 | nC |
| Gate to Source Charge | Q_{gs} | | - | 7.0 | - | nC |
| Gate to Drain "Miller" Charge | Q_{gd} | | - | 22 | - | nC |
| Input Capacitance | C_{ISS} | $V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$ (Figure 11) | - | 1225 | - | pF |
| Output Capacitance | C_{OSS} | | - | 200 | - | pF |
| Reverse-Transfer Capacitance | C_{RSS} | | - | 85 | - | pF |
| Internal Drain Inductance | L_D | Measured from the Contact Screw on Tab to Center of Die | - | 3.5 | - | nH |
| | | Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad | - | 7.5 | - | nH |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | | - | - | 1.0 | $^\circ\text{C/W}$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | Free Air Operation | - | - | 62.5 | $^\circ\text{C/W}$ |



Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|---|-----|-----|-----|-------|
| Continuous Source to Drain Current | I_{SD} | Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode | - | - | 8.0 | A |
| Pulse Source to Drain Current (Note 3) | I_{SDM} | | - | - | 32 | A |
| Source to Drain Diode Voltage (Note 2) | V_{SD} | $T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $V_{GS} = 100\text{A/ s}$ (Figure 13) | - | - | 2.0 | V |
| Reverse Recovery Time | t_{rr} | $T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $dI_{SD}/dt = 100\text{A/ s}$ | 210 | 475 | 970 | ns |
| Reverse Recovered Charge | Q_{RR} | $T_J = 25^\circ\text{C}$, $I_{SD} = 8.0\text{A}$, $dI_{SD}/dt = 100\text{A/ s}$ | 2.0 | 4.6 | 8.2 | C |

NOTES:

2. Pulse Test: Pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive Rating: Pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 14\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 8\text{A}$.

Typical Performance Curves Unless Otherwise Specified

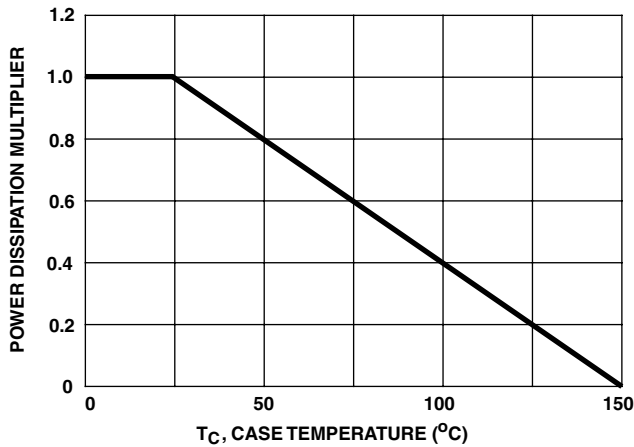


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

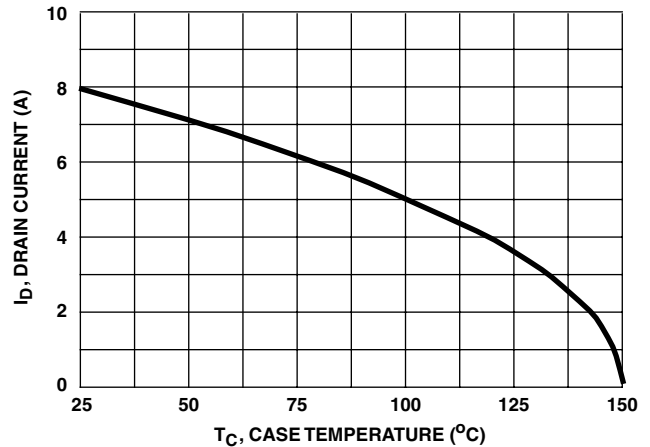


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

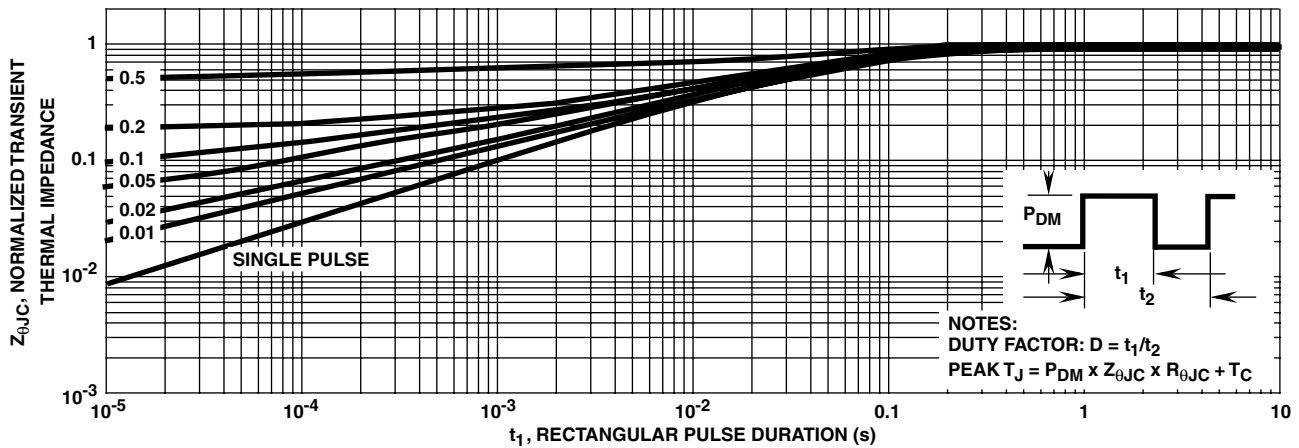


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

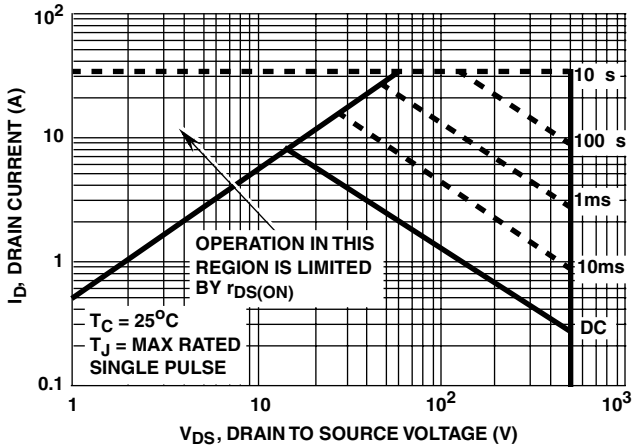


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

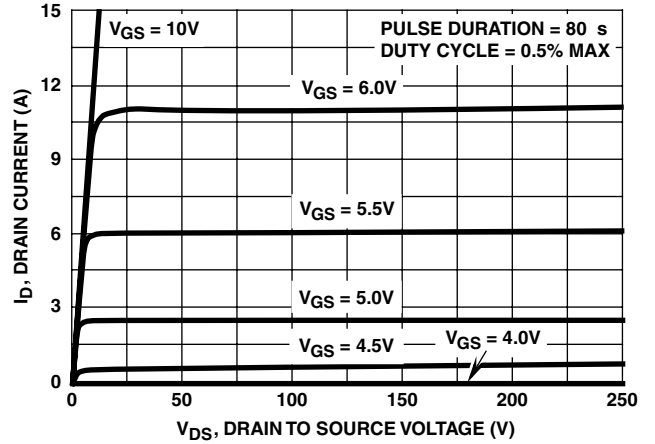


FIGURE 5. OUTPUT CHARACTERISTICS

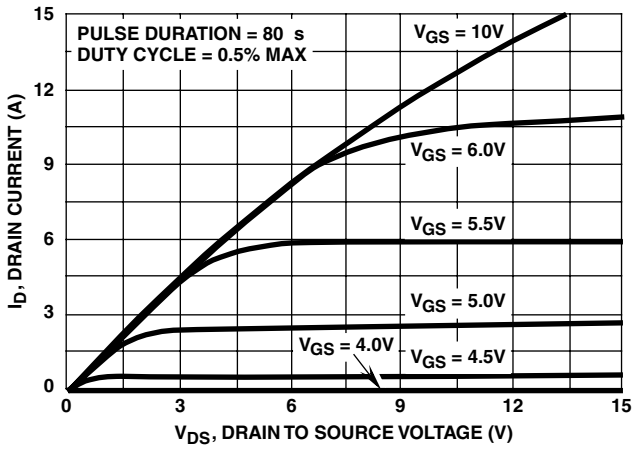


FIGURE 6. SATURATION CHARACTERISTICS

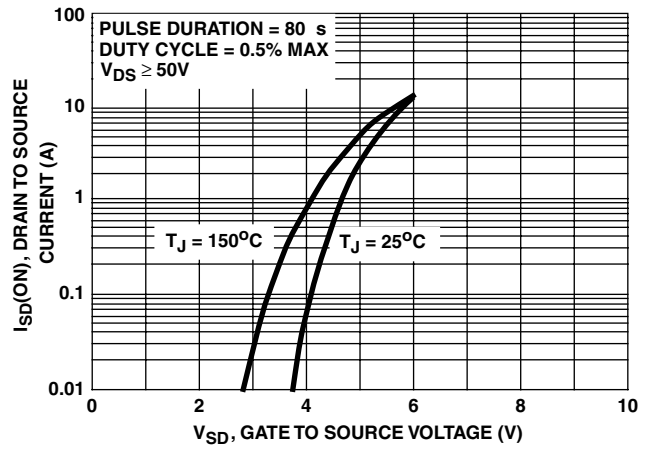


FIGURE 7. TRANSFER CHARACTERISTICS

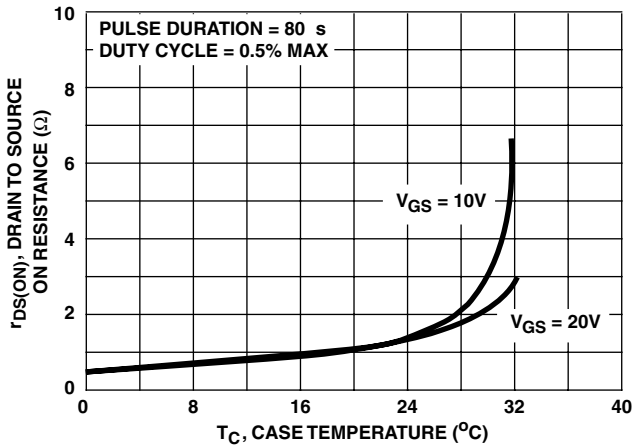


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs VOLTAGE AND DRAIN CURRENT

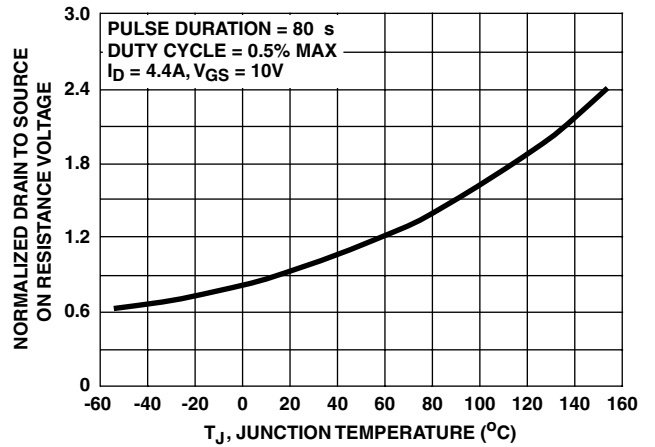


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

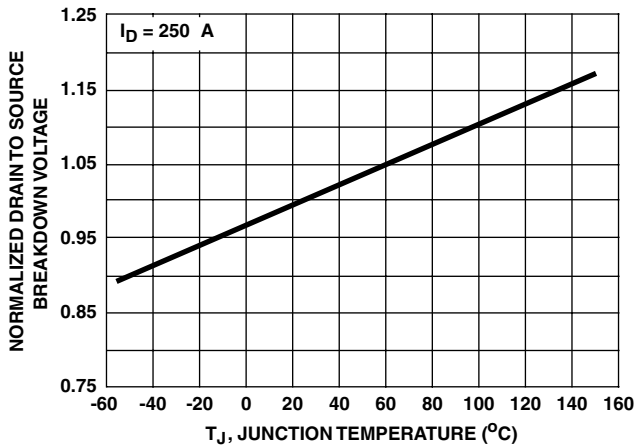


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

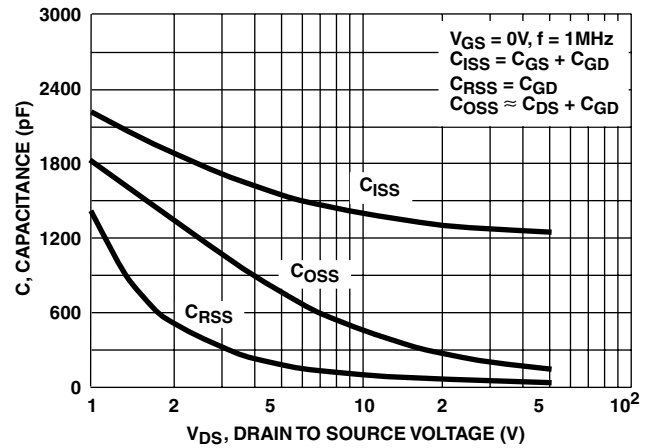


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

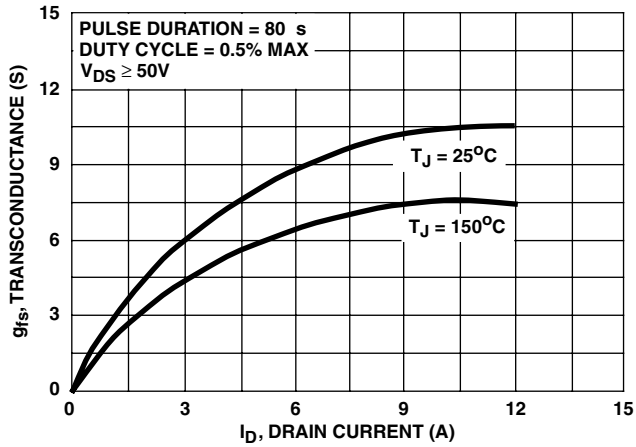


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

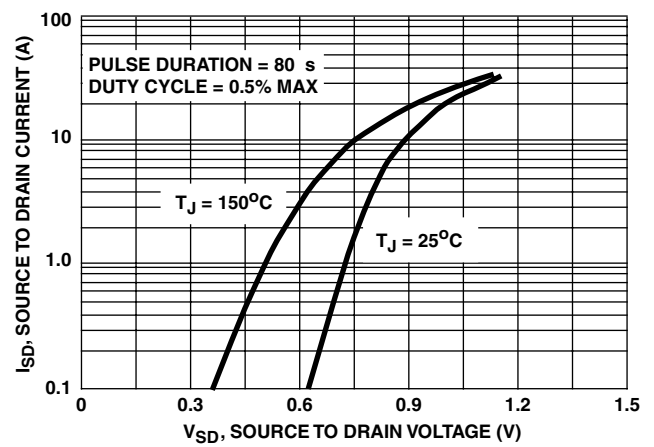


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

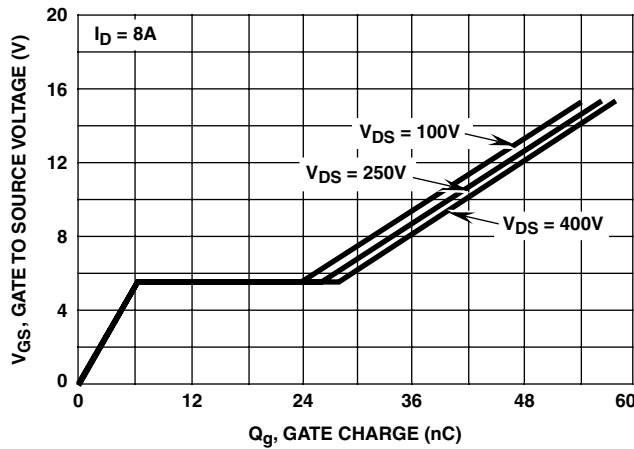


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

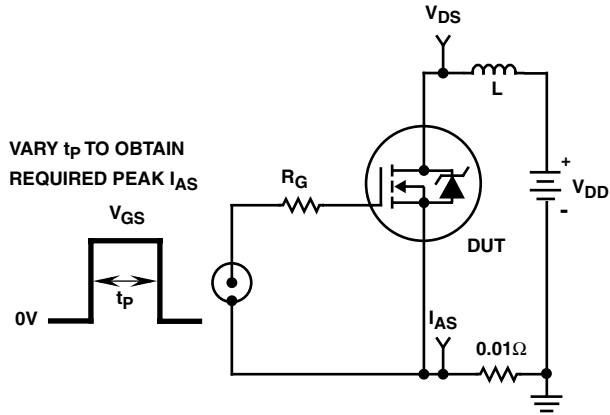


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

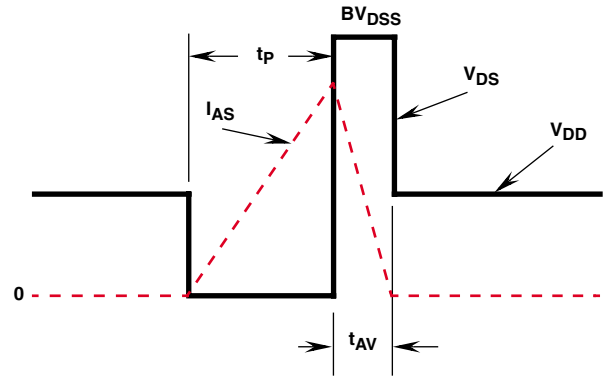


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

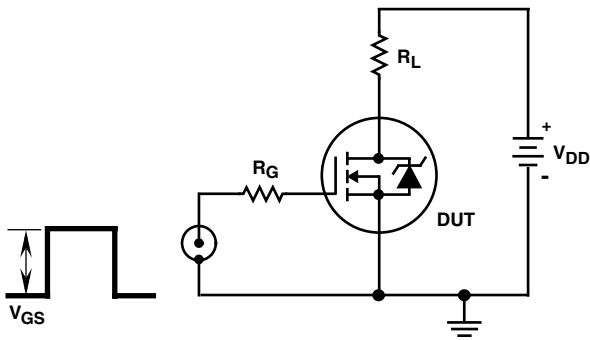


FIGURE 17. SWITCHING TIME TEST CIRCUIT

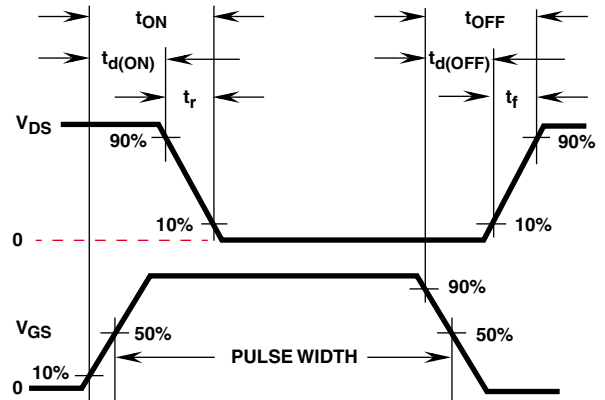


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

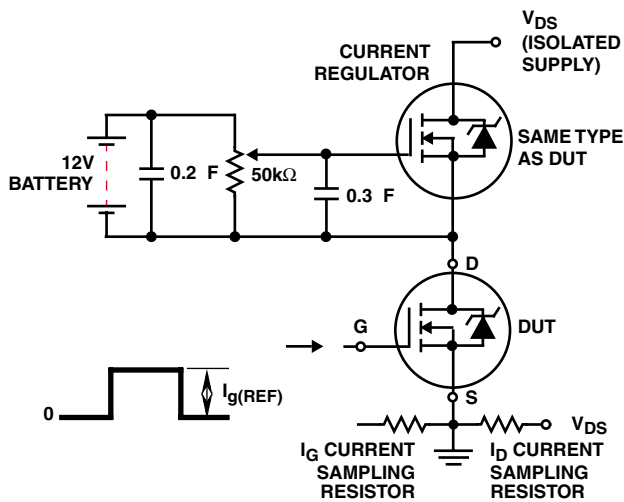


FIGURE 19. GATE CHARGE TEST CIRCUIT

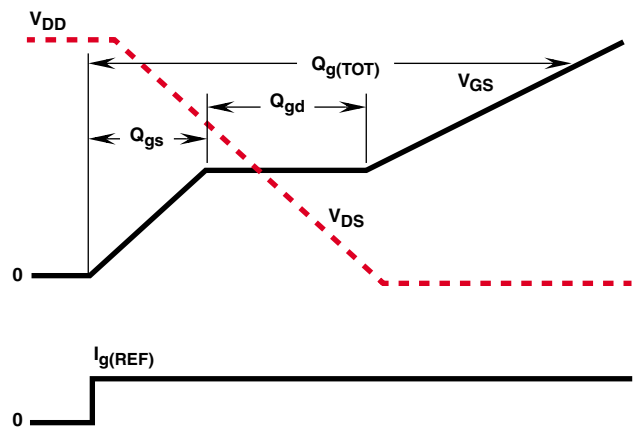


FIGURE 20. GATE CHARGE WAVEFORMS

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

| | | | | |
|----------------------|---------------------|---------------------|-----------------|------|
| ACEx™ | FAST® | OPTOLOGIC™ | SMART START™ | VCX™ |
| Bottomless™ | FASTr™ | OPTOPLANAR™ | STAR*POWER™ | |
| CoolFET™ | FRFET™ | PACMAN™ | Stealth™ | |
| CROSSVOLT™ | GlobalOptoisolator™ | POP™ | SuperSOT™-3 | |
| DenseTrench™ | GTO™ | Power247™ | SuperSOT™-6 | |
| DOME™ | HiSeC™ | PowerTrench® | SuperSOT™-8 | |
| EcoSPARK™ | ISOPLANAR™ | QFET™ | SyncFET™ | |
| E ² CMOS™ | LittleFET™ | QS™ | TinyLogic™ | |
| EnSigna™ | MicroFET™ | QT Optoelectronics™ | TruTranslation™ | |
| FACT™ | MicroPak™ | Quiet Series™ | UHC™ | |
| FACT Quiet Series™ | MICROWIRE™ | SILENT SWITCHER® | UltraFET® | |

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|------------------------|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.